Grenze International Journal of Engineering and Technology, July 2015

An Innovative Method to Reduce Power Consumption using Look-Ahead Clock Gating Implemented on Novel Auto-Gated Flip Flops

Roshini Nair
M.Tech, *MET'S School Of Engineering*, Kerala, India

***Abstract*—Clock gating is extremely useful for decreasing the power wasted by digital circuits. This paper proposes a new and innovative method of look ahead clock gating. It avoids and eliminates the drawbacks of the previously used methods. The existing systems for clock gating are synthesis base clock gating, data driven clock gating and clock gating on auto gated flip flops but all these techniques had a number of disadvantages. This project deals with the elimination of the drawbacks in the existing system Look-Ahead Clock Gating (LACG), combines all the three. LACG computes the clock enabling signals of each FF one cycle ahead of time and further DETFF and dual pulse generator are used to increase performance.**

***Index Terms*— clock gating, clock networks, dynamic power consumption.**

I. INTRODUCTION

The major source of dynamic power consumption in computing and consumer electronics products is the circuit's clock signal. It is responsible for about 30% to 70% of the total switching power consumption [2].Different methods to reduce the dynamic power have been implanted and clock gating is predominant among them. Normally, when a logic unit is clocked, its underlying sequential elements also receives the clock signal no matter whether or not their data will toggle in the next cycle.

Gated clock is a popular method for reducing power dissipation in synchronous digital system. Using this method the clock is not given to the flip flop when the circuit is idle . This considerably reduces the power consumption.

Clock gating is employed at all levels: system architecture, block design, logic design and gates.The most popular is synthesis-based. It derives the clock enabling signals based on the logic of the underlying system,but it leaves the majority of the clock pulses driving the flip-flops (FFs) redundant .To eliminate the problem of redundancy, data-driven clock gating was proposed for flip-flops (FFs).In this method the clock signal driving a FF, is disabled (gated) when the FF's state is not changing in the next clock cycle but it's implementation was extremely complex. The third method called auto-gated FFs (AGFF) is simple but it produces comparatively small power savings. To avoid all these drawbacks a new innovative method of look ahead clock gating was used.

LACG finds the clock enabling signals of each FF one cycle ahead of time.It takes AGFF a leap forward. The main objective of LACG is to reduce the dynamic power consumption, this method is considerably simpler and to improve this technique a novel method of joint gating is used along with this.

Grenze ID: 01.GIJET.1.2.527

II. CLOCK GATING

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. Clock gating works by taking the enable conditions attached to registers, and uses them to gate the clocks. Therefore it is imperative that a design must contain these enable conditions in order to use and benefit from clock gating.

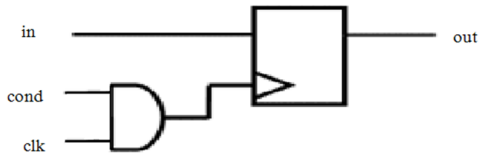

Figure 1 Combinational Clock-Gating

III. EXISTING SYSTEM

Clock gating is a predominant technique used for power saving. It is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. There are mainly three existing methods for clock gating.They are synthesis based clock gating, data-driven method and using auto-gated flip flops.

A. Synthesis-Based Method

Synthesis-based is the most popular method of clock gating. It derives clock enabling signal based on the logic of the underlying system. Normally, when a logic unit is clocked, its underlying sequential elements always gets the clock signal, no matter whether they are toggling in the next cycle. In clock gating, the clock signals are ANDed with already defined enabling signals. Clock gating can be done at all levels: system level, block level, logic level, and gates [2], [3]. Different methods to take advantage of this technique are described in [5]–[7]. These methods are known as synthesis-based methods.

Synthesis-based clock gating is the most popularly used technique by EDA tools [8]. The use of the clock pulses, calculated by using data-to-clock toggling ratio, left after the employment of synthesis-based clock gating can still be very low. These enabling signals were estimated using a mix of logic synthesis and manual definitions. The blocks are arranged in increasing order based on their data-to-clock activity ratio. Due to the rapid increase in design complexity, computer aided design tools are mainly used. Eventhough design productivity is increasing, these tools need the use of a long chain of automatic synthesis algorithms.Unfortunately, these automation gives way to a number of unnecessary clock toggling problems, which furthur increases the number of redundant clock signals at flip-flops (FFs). Synthesis-based method leaves majority of the clock pulses driving the flip-flop redundant. So to overcome this disadvantage other methods have to be used.

B. Data-Driven Method

A data-driven method stops majority of the redundant clock pulses and produces higher power savings. In this the clock signal driving a FF, is disabled at the time when the FF's state is not subject to variation in the next clock cycle[9]. In an effort to decrease the area overhead of gating logic,a number of FFs are controlled by the same clock pulse which is generated by ORing the enabling signals of the individual FFs [8]. Depending on toggling probability, a model to derive the group size maximizing the power savings was made. The results found after comparing both the synthesis-based and data-driven gating methods proved that the latter outperforms for control and arithmetic circuits, while the former outperforms for register-file based circuits [10].

Data-driven gating method is depicted in Fig.2. A FF understands that its clock pulse can be disabled in the next cycle by XORing it's output with the present input data. Furthur the outputs of XOR gates are ORed to produce a joint gating signal for FFs. This is then latched to avoid glitches. The combination of a latch with AND gate is called Integrated Clock Gate (ICG) [5]. It is advantageous to group FFs whose switching activitiy patterns are highly similar. The work in [7] dealt with the questions of which FFs should be placed in a group to maximize the power savings, and how to identify those groups.

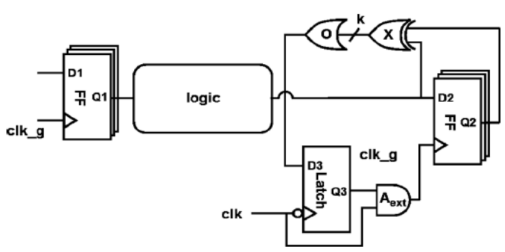

Figure 2 Data Driven Clock Gating

Data-driven method has the disadvantage of very short time-window where the gating circuit can work without any trouble. The overall delay of the XOR, OR, latch and the AND gate should not exceed the setup time of the FF. These constraints may exclude 5%-10% of the FFs from being gated because they are present on critical paths [11].

Along with this drawback data-driven gating also suffers from very complex design methodology. In order to maximize the power savings, the FFs should be grouped in such a way that their toggling activity is highly similar,for this a number of extensive and expensive simulations have to be done. In majority of the cases these applications are unknown and the amount of wasted clock pulses will considerably increase for specific applications.

C. Auto-Gated Flip Flops

Auto-Gated FFs (AGFF) is simple but yields relatively small power savings. In this only the slave flip-flops are gated. The basic circuit used for LACG is Auto-Gated Flip-Flip (AGFF) illustrated in Fig.3 [8]. The FF's master latch becomes transparent on the falling edge of the clock, where its output must stabilize no later than a setup time prior to the arrival of the clock's rising edge, when the master latch becomes opaque and the XOR gate indicates whether or not the slave latch should change its state. If it does not, its clock pulse is stopped and otherwise it is passed.

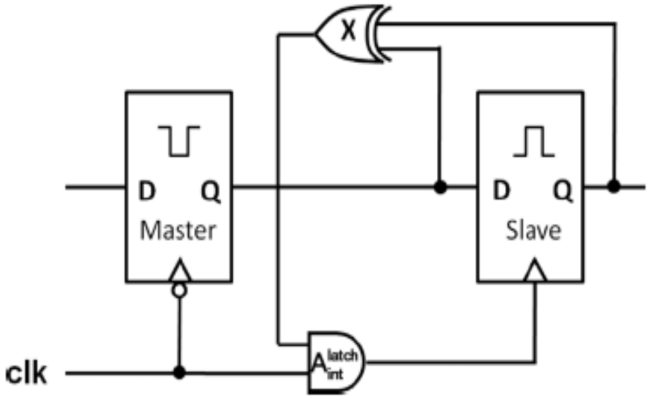

Figure 3 Auto-Gated Flip-Flops

In [8] a significant power reduction was reported for register-based small circuits.AGFF can also be used for general logic, but with major drawbacks. In this only the slave latches are gated ,half of the clock load is not gated, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating and it yields only small power savings.

To avoid these drawbacks that is to decrease the dynamic power consumption, to avoid the tight timing constraints and to save overhead a new innovative technique was needed.

IV. Existing System

LACG computes the clock enabling signals of each FF one cycle ahead of time, based on the present cycle data of those FFs on which it depends. It avoids the tight timing constraints of AGFF and data-driven. LACG takes AGFF a leap forward.

Similarly to data-driven gating, it is capable of stopping the majority of redundant clock pulses.Furthermore, unlike data-driven gating whose optimization requires the knowledge of FFs' data toggling vectors, LACG is independent of those.

LACG is based on using the XOR output in Fig 4 to generate clock enabling signals of other FFs in the system, whose data depend on that FF. There is a problem though. The XOR output is valid only during a narrow window [-tsetup,tccq] of around the clock rising edge, where tsetup and tccq are the FF's setup time and clock to output contamination delay, respectively. After a tccq delay the XOR output is corrupted and turns eventually to zero. To be valid during the entire positive half cycle it must be latched as shown in Fig 4 and Fig 5 is the symbol of the enhanced AGFF with the XOR output. The power consumed by the new latch can be reduced by gating its clock input clk_g.The working of look ahead clock gating by using auto-gated flip flops is shown in Fig 4.

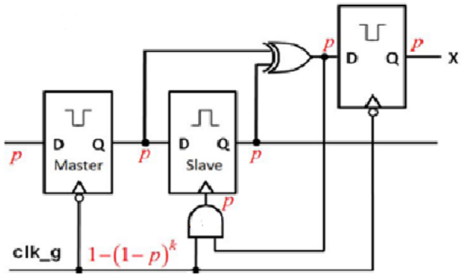

Figure 4 Enhanced AGFF Used For LACG

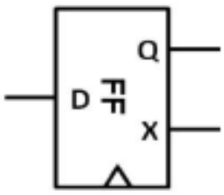

Figure 5 Symbol for enhanced AGFF

A. Working of LACG

Fig 6 illustrates how LACG works. We call FF'' target and FF' source. A target FF depends on K>1 source FFs. It is required that the logic driving a target FF does not have an input externally of the block. Let X(D") denote the set of the XOR outputs of the source FFs, and denote by Q(D") the set of their corresponding outputs. The source FFs can be found by a traversal of the logic paths from D" back to Q(D'').

Using a FF for gating is a considerable overhead that will consume power of its own. This can significantly be reduced by gating FF"' as shown in Fig 6 since FF"' is oppositely clocked and its data is sampled at the clock's falling edge, its clock enabling signal X"' must be negated. Also ,FF"' is an ordinary FF where the internal XOR gate is connected between D"' and Q'".

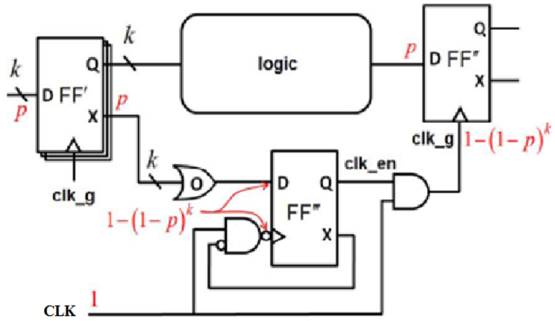

Figure 6 LACG Of General Logic

B. Modeling the Power Savings

While modeling the power Savings independency should not be considered, that is the worst case condition .ratio of toggling probability and source FF s must be kept in mind.to get the reduced power dissipation the power saving break even curve must be analysed.

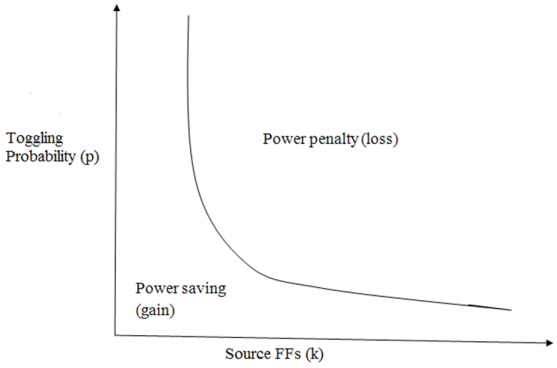

Figure 7 Power Saving Break even Curve

C. Minimizing the Gating Logic

The gating logic can be shared among several target FFs, which further reduces the overhead.Logic sharing model is developed to minimize the gating cost. The idea is illustrated in Fig 14, showing two target FFs, FFi and FFj ,with their corresponding OR trees,driven by ki and kj source FFs, respectively. A different implementation is shown in Fig 15 were the OR logic is merged and a single gater is used for the two FFs.

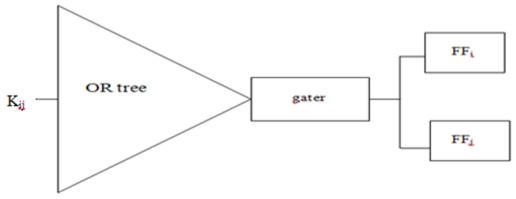

Figure 8 Overlapping OR Gate Logic

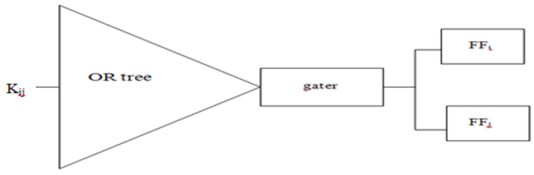

Figure 9 Merging OR Logic For Joint Gating

V. Innovative Method of DETFF

The power consumption of a system is a crucial parameter in modern VLSI circuits especially for low power applications. To further reduce power consumption double edge triggered flip flops are used.
The proposed DETFF is having less number of clocked transistors than existing designs. The most popular synchronous digital circuits are edge triggered flip-flops. The total clock related power consumption in synchronous VLSI circuits is due to power consumption in the clock network, power consumption in the clock buffers, and power consumption in the flip-flops [3].
By using double-edge triggered flip-flops (DETFFs), the clock frequency can be significantly reduced ideally, cut in half while preserving the rate of data processing. A simple DETFF is implemented with about 50% extra transistors than the traditional SET flip flop, however, this issue is also being resolved.
The basic working of a simple DETFF is shown below in figure .In this D is sampled on both rising and falling edges of clock and it doubles data rate per clock edge.During the rising edge of the clock the upper D flip flop will be working and during the falling edge the lower D flip flop will be working and the output will be produced from the multiplexer accordingly.

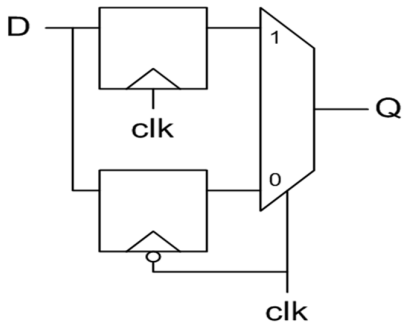

Fig 10 Double Edge Triggered Flip-Flop

VI. New Proposed System

The conventional structures have a number of drawbacks like the increased number of transistors ,increased area overhead and complexity. To avoid all these a new innovative structure of DETFF is used. The proposed Double Edge Triggered Flip-Flop (DETFF) design is shown in Fig. 3. The operation of the proposed flip-flop is similar to that of figure 1, but the number of clocked transistors is reduced from 10 to 6.This is done by replacing the transmission gates by using n-type pass transistors.
As a result the proposed DETFF in figure 6.4 is free from threshold voltage loss problem of pass transistors.Along with this the feedback network of figure 1 is changed by replacing the p-type pass transistor by n-type pass transistor as, the area used by NMOS is less than that of PMOS.Thus the proposed Double Edge Triggered Flip-Flop (DETFF) has become more efficient in terms of area, power and speed.

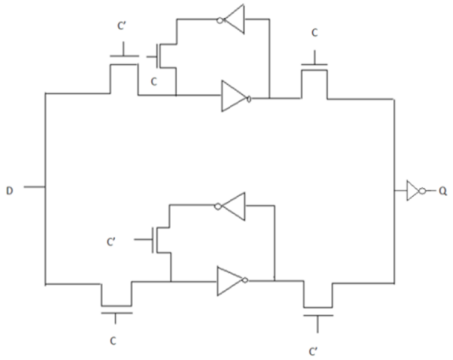

Figure 11 Proposed DETFF

A. Dual Pulse Generator

In this along with the DETFF instead of clock signal a dual pulse generator is used. In dual edge triggering the flip flop is triggered in both edges of clock pulses.Instead, applying the clock signal to the flip flop the dual pulse is applied using dual pulse generator scheme shown in figure 12.Dual pulse generator is integrated with DETFF.

The pulse generator consists of two transmission gates and four inverters shown in figure 20. When clk=1 the upper TG is ON and lower TG if OFF the output pulse=0.

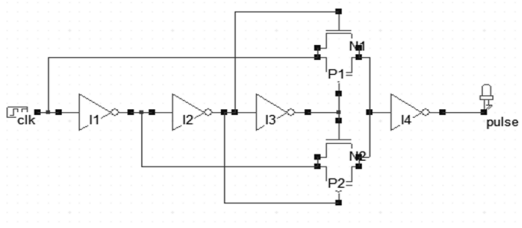

Figure 12 Dual Pulse Generator Circuit

When the clk transit from 1 to 0 suddenly the pulse=1. That is the output of the invertor I3 is '1'. Similarly, when clk=0 the lower TG is responsible to produce the pulse at negative edge of the clock.

VII. Experimental Results

Data driven method, auto-gated flip flops and LACG has been implemented practically and the time period ,area and total estimated power has been compared. In data driven method the minimum time period is around 2.722ns and the gate count is 373 and the total estimated power is around 63. In the method using auto gated flip flops the time required will be less around 2.452 ns and gate count will be considerably reduced to 44 and the estimated power will be 48, but this method cannot be implemented practically in large circuits so it is not preferable so we opt for LACG .In LACG the time period will be around 2.245ns and the number of gates will be 218 and the total estimated power will be 47 and maximum power reduction is obtained in LACG. So the flip flops in LACG is replaced by DETFF which further reduces the power dissipation by 30-40%.

VIII. Conclusion

One of the major sources responsible for dynamic power consumption is the system's clock signal. Earlier different methods of clock gating was used to reduce power consumption due to the clock signals. The main methods were synthesis based method, data-driven method and clock gating using auto-gated flip-flops ,but all these methods had certain drawbacks. To avoid these drawbacks the look-ahead clock gating method on auto-gated flip-flops was adopted. The gating logic in this is further optimized by joint gating which reduces the hardware overheads. The power dissipation and area is further reduced using DETFF in place of D flip flops in LACG.

References

[1] L. Benini, A. Bogliolo, and G. De Micheli, "A survey on design techniques for system- level dynamic power management," IEEE Trans.VLSI Syst., vol. 8, no.3, Jun. 2000.

[2] M. S. Hosny and W. Yuejian, "Low power clocking strategies in deepsubmicron technologies," in Proc. IEEE Int. Conf. Integr. Circuit DesignTechnol., ICICDT 2008,

[3] C. Chunhong, K. Changjun, and S. Majid, "Activity-sensitive clocktree construction for low power," in Proc. ISLPED, 2002,

[4] A. Farrahi, C. Chen, A. Srivastava, G. Tellez, andM. Sarrafzadeh, "Activity-driven clock design," IEEE Trans. Comput. Aided Des. Integr.Circuits Syst., vol. 20, no. 6, 2001.

[5] W. Shen, Y. Cai, X. Hong, and J. Hu, "Activity and register placement aware gated clock network design," in Proc. ISPD, 2008.

[6] S. Wimer and I. Koren, "The Optimal fan-out of clock network for power minimization by adaptive gating," IEEE Trans. VLSI Syst., vol.20, no. 10,Oct. 2012.

[7] S. Wimer and I. Koren, "Design flow for flip-flop grouping in data driven clock gating," IEEE Trans. VLSI Syst., to be published.
[8] 8 J. Oh and M. Pedram, "Gated clock routing for low-power microprocessor design," IEEE Trans. Comput.-Aided Design Integr. CircuitsSyst., vol. 20, no. 6,Jun. 2001
[9] A. G. M. Strollo and D. De Caro, "Low power flip-flop with clock gating on master and slave latches, " , Electron.Lett., vol. 36, no. 4 Feb. 2000
[10] Xiaowen Wang and William H. Robinson, "A Low-Power Double Edge-Triggered Flip-Flop with Transmission Gates and Clock Gating," IEEE Conference, pp 205-208, 2010.
[11] Yu Chien-Cheng,, "Low-Power Double Edge- Triggered Flip-Flop Circuit Design," Third International Conference on Innovative Computing Information and Control (ICICIC'08), IEEE Conference, 2008.
[12] J. Kathuria, M. Ayoub, M. Khan, and A. Noor, "A review of Clock Gating Techniques," MIT Int. J. Electron. and Commun. Engin., vol.1, no. 2,Aug. 2011.
[13] S. Wimer, "On optimal flip-flop grouping for VLSI power minimization,"Oper. Res. Lett., vol. 41, no. 5, Sep. 2013.
[14] C. Chunhong, K. Changjun, and S. Majid, "Activity-sensitive clocktree construction for low power," in Proc. ISLPED, 2002

AUTHOR

Roshini Nair, is a M. Tech (VLSI) scholar of MET's School of Engineering. A very proactive student,she has passed her B.Tech from University of Calicut, Kerala (First Class With Honours), She has received many honours and commendations for her presentations and publications. Her keen interest in conceiving and designing low power, high speed integrated circuits and systems has motivated her to innovate new tools and techniques for addressing problems in High Performance Computing Architectures. She is ardently dedicated to Research and Development work to develop integratable low power circuits from the point of VLSI product design.